Code :ECT3224

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**III B.Tech II Semester(R05) Supplementary Examinations, April/May 2011**
**COMPUTER ORGANIZATION**
**(Electronics & Control Engineering)**
**(For students of RR regulation readmitted to III B.Tech II Semester R05)**

**Time: 3 hours** **Max Marks: 80**

**Answer any FIVE questions**
**All questions carry equal marks**

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1. Explain about VonNeumann architecture design in detail.
2. (a) What is BCD representation. List the advantages of it.
   (b) Convert the following binary numbers to decimal and octal forms
      i. 101101110
      ii. 1.011101
3. (a) What is big-endian and little-endian address mapping
   (b) List points favoring big-endian and little-endian styles.
   (c) What is bit ordering?
4. (a) List the characteristics of superscalar processors and contrast it with CISC processors.
   (b) Explain the instruction execution characteristics of RISC processors.
   (c) What is semantic gap problem?
5. (a) What is demand paging. Explain it's advantages and disadvantages.
   (b) Explain the page table structure. Discuss it's purpose.
6. (a) Elaborate about purpose and organization of data on magnetic tap.
   (b) Differentiate between magnetic-disk and magnetic-tape systems.
   (c) Discuss the technology used for CD-ROM systems.
7. (a) List sequencing and branching control fields of IBM 3033 microinstruction.
   (b) Discuss the functioning of micro sequencer with example.
8. A pipelined processor has two branch delay slots. An optimizing complier can fill one of these slots 85 percent of the time and can fill second slot only 20 percent of the time. What is the percentage improvement in performance achieved by this optimization?

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